REMARKS

Claims 1-34 are pending in the application. Claims 1-34 have been rejected. Claims 5, 6, 11, 12, and 13 have been amended to correct minor informalities. Reconsideration of the Claims is respectfully requested.

1. Information Disclosure Statement

The examiner stated that the" Information Disclosure Statement filed January 20, 2004 failed to comply with 37 CFR 1.98(a)(2) which requires a legible copy of each U.S. and foreign patent . . ."

Applicants hereby resubmit the "missing documents" previously sent with the January 20, 2004 Information Disclosure Statement. Applicants have also resubmitted a clean copy of pages 1-7, 2-7, 4-7, and 6-7 of the Information Disclosure Statement by Applicant to aid the examiner in returning to Applicants an initialed copy.

2. Oath/Declaration

> The Office Action states:
> The oath or declaration is defective because:
> It does not identify the mailing address of each inventor.... The mailing address may be provided in an application data sheet or supplemental oath or declaration.

Applicants submitted the Declaration in compliance with 37 CFR 1.63 at the time of filing the application on February 27, 2002. Further, Applicants also submitted at the time of filing an Application Data Sheet that included the above requested information. Applicants have attached hereto a copy of both the Declaration and the Application Data Sheet as filed. Therefore, the Declaration in this application is not defective and complies with all Patent Office rules.

3. Drawings

The drawings have been objected to because of inconsistencies and informalities. Replacement sheets have been provided correcting the inconsistencies and informalities to overcome the objection. No new matter has been added.

AMENDMENTS TO THE DRAWINGS

The attached Replacement Sheets of drawings includes changes to Fig. 1, Fig. 6, and Fig. 8. The attached sheets replace the original sheet containing Fig. 1, Fig. 6, and Fig. 8.

For Fig. 1, the attached sheet changes the number "132" to "128", and the number "128" to "132".

For Fig. 6, the attached sheet adds the term "REQ (ADDRESS)" to the dashed signal line between Master 1 and the Bus Arbiter. Additionally, "656" was shown with two lead lines. Accordingly, one of the two lead lines was deleted.

For Fig. 8, the reference sign "800" was added, which is supported by the specification.

No new matter has been added by this amendment

4. Specification

The Specification was object objected to due to informalities. Appropriate corrections have been made to overcome the objection. No new matter has been added.

5. Rejection under 35 U.S.C. § 102(b)

The Office Action had rejected (i) claims 5-6 and 19, (ii) claims 10-12, 14-15, and 17, and (iii) claims 30-34 under 35 U.S.C. 102(b).

"'A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' . . . 'The identical invention must be shown in as complete detail as is contained in the . . . claim.' The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, *i.e.*, identity of terminology is not required." See MPEP § 2131, p. 2100-73 (May 2004) (citations omitted).

(i) Claims 5-6 and 19 were rejected under 35 U.S.C. 102(b) as being anticipated by Billings et al. (U.S. Patent No. 5,867,694) ("Billings"). Applicant respectfully traverses this rejection.

Billings recites an "invention [that] relates to information handling systems and, more particularly, to information handling systems having means for controlling a number of clocks operating at different frequencies." (Billings 1:10-13).

Applicant's claim 5, as amended, recites "[a] method for generating sample cycle pulses, comprising: determining a ratio of an internal clock of a device to the clock of a bus; and generating a sample cycle pulse in an appropriate cycle of the internal clock with respect to the ratio."

Applicant's claim 19, as amended, recites "[a] bus slave, comprising: at least one input port for receiving communication signals and control signals; circuitry for determining a bus frequency; circuitry for determining a ratio between an internal clock of the bus slave and the bus frequency; and circuitry for determining when to latch a communication signal being received over the at least one input port with respect to the ratio."

In contrast, Billings provides a "clock generation circuit which can be used to generate bus clocks with required . . . cycle skews without a requirement for distributing separate clocks on an integrated circuit chip." (Billings 4:15-18).

Billings does not set forth, *inter alia*, "circuitry for determining when to latch a communication signal being received over the at least one input port with respect to the ratio", nor " generating a sample cycle pulse in an appropriate cycle of the internal clock with respect to the ratio ." Accordingly, each and every element as set forth in the claim is not found, either expressly or inherently described, in Billings. Applicant respectfully requests that the rejection of its Independent Claim 5 and Claim 6, which depends from Claim 5, and Claim 19, be withdrawn.

(ii) Claims 10-12, 14-15, and 17 were rejected under U.S.C. 102(b) as being anticipated by Kelley et al. (U.S. Patent No. 6,134,621) ("Kelley"). Applicant respectfully traverses this rejection.

Kelly recites an "invention [that] relates generally to information processing systems and more particularly to varying bus speeds in accordance with slot configurations for PCI systems." (Kelley 1:5-8).

Applicant's Claim 10, as amended, recites "[a] method for selecting a bus frequency, comprising: setting a bus frequency according to a transaction having a source and a destination, the bus frequency being such that the device receiving a communication of the transaction will have a frequency that is an integer multiple of the bus frequency."

In contrast, Kelly recites the use of "M66EN signals [that] are PCI specified signals and are representative of the frequency at which a plugged-in PCI device is capable of running. For example, if "1M66EN" is at a zero or low logic level with a device plugged-onto slot #1 117, then the device is capable of running at only 33 MHz. However, if the 1M66EN is at a high logic level, then . . . the device is capable of running at 66 MHz." (Kelley 2:38-45). In other words, the pins-outs of the PCI card indicate the use of the 33 MHz rate.

That is, Kelley does not provide, *inter alia*, setting a bus frequency according to a transaction . . . ." Accordingly, each and every element as set forth in the claim is not found, either expressly or inherently described, in Kelley. Applicant respectfully

requests that the rejection of its Independent claim 10 and claims 10-12, 14-15, and 17, which depend either directly or indirectly there from, be withdrawn.

(iii) Claims 30-34 were rejected under 35 U.S.C. 102(b) as being anticipated by Solomon (U.S. Patent No. 5,943,483) ("Solomon").

Solomon recites "an improved method and apparatus for transferring data across a bus in a data processing system. Still more particularly . . . a method and apparatus for transferring data across a bus using intelligent bus arbitration."

Applicant's claimed invention of Claim 30, as amended, recites "[a] system, comprising: a port; a bus; a bus master coupled between the port and the bus; a processor coupled to the bus; and a memory device coupled to the bus, wherein the memory device comprises a memory portion storing data that defines arbitration logic and clock generation logic for the bus."

In contrast, Solomon does not provide, *inter alia*, the "memory portion storing data that defines arbitration logic and clock generation logic for the bus" of Applicant's claimed invention. Accordingly, each and every element as set forth in the claim is not found, either expressly or inherently described, in Solomon. Applicant respectfully requests that the rejection of its Independent claim 30 and claims 31-34, which depend either directly or indirectly there from, be withdrawn.

6. Rejection under 35 U.S.C. § 103(a)

The Office Action had rejected (i) claims 1-4, 16, and 21-26, (ii) claims 7 and 9, (iii) claim 8, (iv) claim 13, (v) claim 18, (vi) claim 20, (vii) claim 27, (viii) claim 28, and (ix) claim 29 under 35 U.S.C. 103(a).

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*,

947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). MPEP § 2142, p. 2100-128 (Rev. 2, May 2004).

These rejections are respectfully traversed in that, as shown below, there is no suggestion or motivation to combine the references to achieve Applicant's claimed invention. Further, it is respectfully submitted that in several instances Applicant's specification is used as a blue print in an attempt to bring disassociated references having no suggestion or motivation to combine, serving as an improper basis for rejection of Applicant's claimed invention.

(i) Claims 1-4, 16, and 21-26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Solomon and Kelley. Applicant respectfully traverses these rejections.

Solomon recites "an improved method and apparatus for transferring data across a bus in a data processing system. Still more particularly . . . a method and apparatus for transferring data across a bus using intelligent bus arbitration."

Kelly recites an "invention [that] relates generally to information processing systems and more particularly to varying bus speeds in accordance with slot configurations for PCI systems." (Kelley 1:5-8). In other words, Kelley relies on PCI card pin-outs for toggling between a 66 MHz and a 33 MHz bus rate.

Claim 1 as amended, sets out "[a] bus arbiter coupled to a first and second bus master, a first and second slave and a bus, comprising: at least one port coupled to receive bus request commands for a transaction from either the first or second bus master and coupled to receive an address or identity of the first and second slaves for the transaction, and also coupled to communicate over the bus; and logic circuitry that defines logic to select a bus frequency according to the requested transaction."

Accordingly, there is no suggestion or motivation, in either retry arbiter of Solomon or the PCI pin-out apparatus of Kelley, to modify or combine them to achieve Applicant's Claim 1, which comprises, *inter alia*, "logic circuitry that defines logic to select a bus frequency according to the requested transaction. Applicant respectfully requests that the rejection of its Independent claim 1 and claims 3-4, which depend either directly or indirectly there from, be withdrawn.

Claim 16 depends from Claim 10, and accordingly, incorporates the limitations of Claim 10, as amended. As respectfully set out above, Applicant's Claim 10, as amended, is not anticipated by Kelley. It appears that the combination of Kelley in view of Solomon was tendered in view of Solomon's recitation of "bus arbitration," but Solomon sets out an "arbiter 212 [that] provides intelligent arbitration that provides for an intelligent retry behavior . . . ." (Solomon, col. 34-37). There is no suggestion or motivation, in either Solomon or Kelley, to modify or combine them to achieve Applicant's Claim 16, which depends from independent Claim 10. Applicant respectfully requests that the rejection of its claim 16 be withdrawn.

Claim 21 as amended recites "[a] system, comprising: first and second bus masters; first and second slaves; a bus coupled to the first and second bus masters and the first and second slaves; and a bus arbiter coupled to the bus, the bus arbiter comprising: at least one port coupled to receive bus request commands for a transaction from either the first or second bus master and coupled to receive an address or identity of the first and second slaves for the transaction, and also coupled to communicate over the bus; and logic circuitry that defines logic to select a bus frequency according to the requested transaction."

There is no suggestion or motivation, in either Solomon or Kelley, to modify or combine them to achieve Applicant's Claim 21, which comprises, *inter alia*, "logic circuitry that defines logic to select a bus frequency according to the requested transaction. Applicant respectfully requests that the rejection of its Independent claim 21 and claims 22-24, which depend either directly or indirectly there from, be withdrawn.

(ii) Claims 7 and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Billings as applied to claims 5-6, and further in view of Summer, Jr. et al. (U.S. Patent No. 4,414,624) ("Summer"). Applicant respectfully traverses this rejection.

Billings recites an "invention [that] relates to information handling systems and, more particularly, to information handling systems having means for controlling a number of clocks operating at different frequencies." (Billings 1:10-13). Billings provides a "clock generation circuit which can be used to generate bus clocks with

required . . . cycle skews without a requirement for distributing separate clocks on an integrated circuit chip." (Billings 4:15-18). That is, a device for skewing bus cycles.

Summer recites a "concept [involving] partition the trainer program into modules and dedicating the processing of each module to a separate microcomputer. A group of identical microcomputers execute the total program in an intrinsically parallel mode within the frame times scheduled by a system state control microcomputer." (Summer 2:10-16). That is, a concept for training.

Claims 7, as amended, recites "[a] method for communicating over a bus, comprising: generating a request for access or control of the bus, which request is generated by a bus master; determining a bus frequency being set by a bus arbiter; receiving a grant from the bus arbiter indicating that the bus master may take control of the bus; commencing a transaction at a frequency that matches the bus frequency; comparing an internal clock frequency to the clock frequency of the bus; generating an internal sample cycle signal signals; whenever a sample cycle signal is generated, latching data on the bus; and upon termination of the transaction, issuing a release signal to release the bus to allow a resource of the bus to be available for a subsequent transaction.

There is no suggestion or motivation, in either the skew-shift technique of Billings or the trainer concept of Summer, to modify or combine them to achieve Applicant's Claim 7, which comprises, *inter alia*, "determining a bus frequency being set by a bus arbiter; receiving a grant from the bus arbiter indicating that the bus master may take control of the bus; commencing a transaction at a frequency that matches the bus frequency . . . ." (Claim 7). Applicant respectfully requests that the rejection of its Independent claim 7 and claim 9, which depends either directly or indirectly there from, be withdrawn.

(iii) Claim 8 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Billings as applied to Claim 18, and further in view of Ogletree (U.S. Patent No. 5,579,477) ("Ogletree"). Applicant respectfully traverses this rejection.

Butler recites an apparatus "comprising first and second redundant periodic generators, such as oscillators, having nominally equal frequencies." (Butler 3:10-15). That is, Butler relates to oscillator sources.

Claim 8 depends from Claim 7, and incorporates the limitations set forth therein. In view of the lack of suggestion or motivation, in either the skew-shift technique of Billings or the trainer concept of Summer, to modify or combine them to achieve Applicant's Claim 7, these references similarly lack any suggestion or motivation, including Butler's oscillation apparatus, to modify or combine these references to achieve Applicant's Claim 8. Applicant respectfully request that the rejection of claim 8 be withdrawn.

(iv) Claim 13 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Kelley, and further in view of Lee et al. (U.S. Patent No. 6,611,893) ("Lee"). Applicant respectfully traverses this rejection.

Kelley recites an "invention [that] relates generally to information processing systems and more particularly to varying bus speeds in accordance with slot configurations for PCI systems." (Kelley 1:5-8). Kelly also recites the use of "M66EN signals [that] are PCI specified signals and are representative of the frequency at which a plugged-in PCI device is capable of running. For example, if "1M66EN" is at a zero or low logic level with a device plugged-onto slot #1 117, then the device is capable of running at only 33 MHz. However, if the 1M66EN is at a high logic level, then . . . the device is capable of running at 66 MHz." (Kelley 2:38-45). In other words, the pins-outs of the PCI card indicate the use of the 33 MHz rate.

Lee recites an "invention [that] pertains to arbitration of access to an electronic bus." (Lee 1:7-10). Lee also recites having "knowledge of the speed and phase of the clock of each of the core devices that utilizes the bus, such as by storing that information in a look up table." (Lee 3:49-52).

Claim 13 recites "further comprising determining the identity of the devices in the transaction and examining a table to determine a corresponding bus frequency." Claim 13 depends from Claim 10, and incorporates the limitations set forth therein. Neither the PCI pin-out technique of Kelley nor the core device knowledge table of Lee provide any suggestion or motivation to modify or combine them to achieve Applicant's claimed invention of Claim 13. Applicant respectfully request that the rejection of claim 13 be withdrawn.

(v) Claim 18 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Kelley and Solomon as applied to Claim 16, and further in view of Eikill et al. (U.S. Patent No. 5,131,085) ("Eikill"). Applicant respectfully traverses this rejection.

Solomon recites "an improved method and apparatus for transferring data across a bus in a data processing system. Still more particularly . . . a method and apparatus for transferring data across a bus using intelligent bus arbitration."

Kelly recites an "invention [that] relates generally to information processing systems and more particularly to varying bus speeds in accordance with slot configurations for PCI systems." (Kelley 1:5-8). In other words, Kelley relies on PCI card pin-outs for toggling between a 66 MHz and a 33 MHz bus rate.

Eikill recites "arrangements for distributing control of the data bus among the devices sharing it." (Eikill 1:10-11). Eikill was proffered for the premise that "Eikill teaches that bus arbitration can be performed by individual bus masters." (Office Action, p. 12, para. 21).

Claim 18 depends from Claim 10, and accordingly, incorporates the limitations of Claim 10, as amended. As respectfully set out above, Applicant's Claim 10, as amended, is not anticipated by Kelley. It appears that the combination of Kelley in view of Solomon was tendered in view of Solomon's recitation of "bus arbitration," but Solomon sets out an "arbiter 212 [that] provides intelligent arbitration that provides for an intelligent retry behavior . . . ." (Solomon, col. 34-37). The addition of Eikill adds no suggestion or motivation lacking in Solomon or Kelley to modify or combine these references to achieve Applicant's claimed invention of Claim 18, which depends from independent Claim 10. Applicant respectfully requests that the rejection of its claim 18 be withdrawn.

(vi) Claim 20 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Billings as applied to Claim 19, and further in view of Ogletree (U.S. Patent No. 5,579,477) ("Ogletree"). Applicant respectfully traverses this rejection.

Billings recites an "invention [that] relates to information handling systems and, more particularly, to information handling systems having means for controlling a

number of clocks operating at different frequencies." (Billings 1:10-13). Billings has a "clock generation circuit which can be used to generate bus clocks with required . . . cycle skews without a requirement for distributing separate clocks on an integrated circuit chip." (Billings 4:15-18).

Ogletree recites using "a processor for controlling the print engine responsive to data from a computer . . . . The present invention provides a significant advantage . . . in that the memory is tested at normal operating speeds, independent of the processor, which provides a more robust the printer memory . . . ." (Ogletree 1:55-67, 2: 1-9)

Claim 20 depends from Claim 19, and accordingly, incorporates the limitations of Claim 19, as amended. As respectfully set out above, Applicant's Claim 19, as amended, is not anticipated by Billings. With respect to the present rejection, it appears that the hypothetical combination of Billings in view of the Ogletree was tendered in view of Ogletree's recitation of a state machine that provides a clock signal. (*see* Office Action, p. 13, para. 22; Ogletree 7:10-33, 5:9-11).

The Applicant's Claim 20 recites "[t]he bus slave of claim 19 further including a state machine for generating a sample cycle signal, the sample cycle signal for prompting the slave to latch the communication signals as a part of determining when to latch communication signals."

There is no suggestion or motivation to modify or combine the cycle skew of Billings with the printer test of Ogletree to archive Applicant's Claim 20, which depends from independent Claim 19, as amended. Applicant respectfully requests that the rejection of its claim 20 be withdrawn.

(vii) Claim 27 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Solomon and Kelley as applied to Claim 26, and further in view of Ghori (U.S. Patent No. 6,243,772) ("Ghori"). Applicant respectfully traverses this rejection.

Solomon recites "an improved method and apparatus for transferring data across a bus in a data processing system. Still more particularly . . . a method and apparatus for transferring data across a bus using intelligent bus arbitration." (Solomon 1:7-12).

Solomon recites an "arbiter 212 [that] provides intelligent arbitration that provides for an intelligent retry behavior . . . ." (Solomon, col. 34-37).

Kelly recites an "invention [that] relates generally to information processing systems and more particularly to varying bus speeds in accordance with slot configurations for PCI systems." (Kelley 1:5-8). In other words, Kelley relies on PCI card pin-outs for toggling between a 66 MHz and a 33 MHz bus rate.

Ghori recites a "method and apparatus for incorporating an appliance into a computer system." (Ghori 1:7-9).

Claim 27 depends indirectly from Claim 21, and accordingly, incorporates the limitations of Claim 21 and interceding claims. The Applicant's Claim 27 recites "[t]he system of Claim 26, wherein the bus arbiter includes dedicated hardware logic that performs table lookup and arbitration tasks." Ghori was proffered as "an ASIC can use look-up tables stored in memory to assist in performing table lookup tasks." (Office Action, p. 13, para. 23). But there is no suggestion or motivation to modify or combine the disjointed references of Solomon, Kelley, and Ghori achieve Applicant's Claim 27, which depends indirectly from independent Claim 21, as amended. Applicant respectfully requests that the rejection of its claim 21 be withdrawn.

(viii) Claim 28 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Solomon and Kelley as applied to Claim 21, and further in view of Billings as applied to claim 19. Applicant respectfully traverses this rejection.

Solomon recites "an improved method and apparatus for transferring data across a bus in a data processing system. Still more particularly . . . a method and apparatus for transferring data across a bus using intelligent bus arbitration." (Solomon 1:7-12). Solomon recites an "arbiter 212 [that] provides intelligent arbitration that provides for an intelligent retry behavior . . . ." (Solomon, col. 34-37).

Kelly recites an "invention [that] relates generally to information processing systems and more particularly to varying bus speeds in accordance with slot configurations for PCI systems." (Kelley 1:5-8). In other words, Kelley relies on PCI card pin-outs for toggling between a 66 MHz and a 33 MHz bus rate.

Billings recites an "invention [that] relates to information handling systems and, more particularly, to information handling systems having means for controlling a

number of clocks operating at different frequencies." (Billings 1:10-13). It provides a "clock generation circuit which can be used to generate bus clocks with required . . . cycle skews without a requirement for distributing separate clocks on an integrated circuit chip." (Billings 4:15-18).

Claim 28 depends indirectly from Claim 21, and accordingly, incorporates the limitations of Claim 21. As set out with respect to Claim 21, neither Solomon or Kelley provide any suggestion or modification to combine them to achieve Applicant's Claim 21, as amended, which comprises, *inter alia*, "logic circuitry that defines logic to select a bus frequency according to the requested transaction.

Billings was relied on for the "slave claimed in dependent claim 28." (Office Action, p. 14, para. 24). The language relied upon by the Office Action recites the problem of "fractional clock speed ratios." (Billings 1: 61-67).

The Applicant's Claim 28 recites "[t]he system of Claim 21, wherein the first slave comprises: at least one input port for receiving communication signals and control signals from the bus; circuitry for determining a bus frequency, circuitry for determining a ration between an internal clock of the bus slave and the bus frequency; and circuitry for determining when to latch communication signals being received over the at least one input port."

There is no suggestion or motivation to modify or combine the retry arbiter of Solomon with the PCI pin-out architecture of Kelley, with the skew compensation scheme of Billings to archive Applicant's Claim 28. Applicant respectfully requests that the rejection of its claim 28 be withdrawn.

(ix) Claim 29 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Solomon, Kelley, and Billings as applied to Claim 20, and further in view of Ogletree as applied to Claim 20 above. Applicant respectfully traverses this rejection.

Claim 29 depends from Claim 28, and depends indirectly to claim 21. Applicant reiterates the lack of suggestion or motivation to suggestion or motivation to modify or combine the retry arbiter of Solomon with the PCI pin-out architecture of Kelley, with the skew compensation scheme of Billings to archive Applicant's Claim 28.

With respect to Claim 29, the Office Action submits the further hypothetical combination of Solomon, Kelley, and Billings, to add the further tenuous element of the

printer test of Ogletree as the basis of its rejection to Applicant's Claim 29. In view of the lack of suggestion or motivation for the first three references, the addition of Ogletree does not cure the lack of prima facie case of obviousness. Applicant respectfully requests that the rejection of its claim 29 be withdrawn.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicants' attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on January 21, 2005.

Pat Slaback
Name

Signature